

1/6

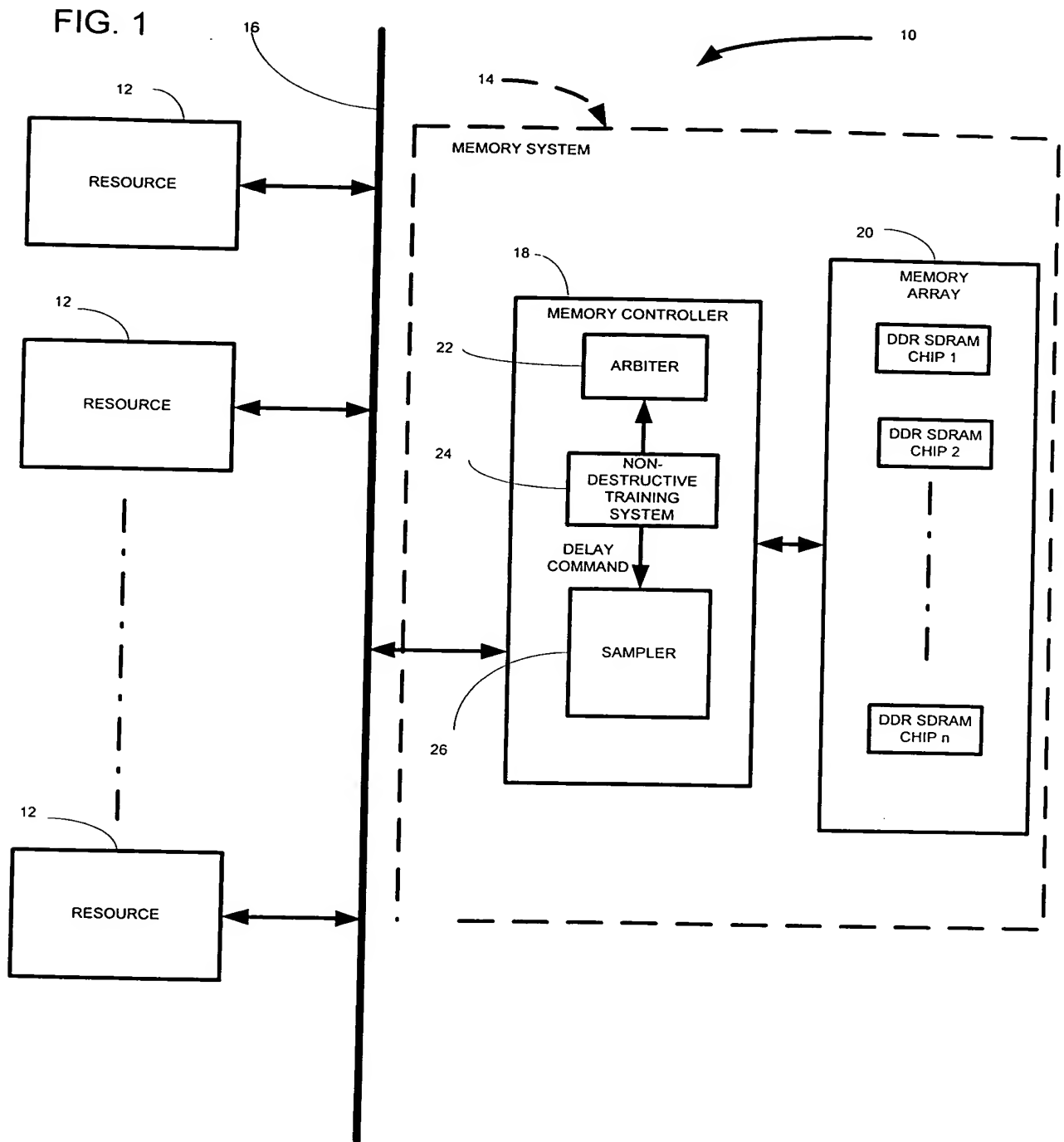


FIG. 2

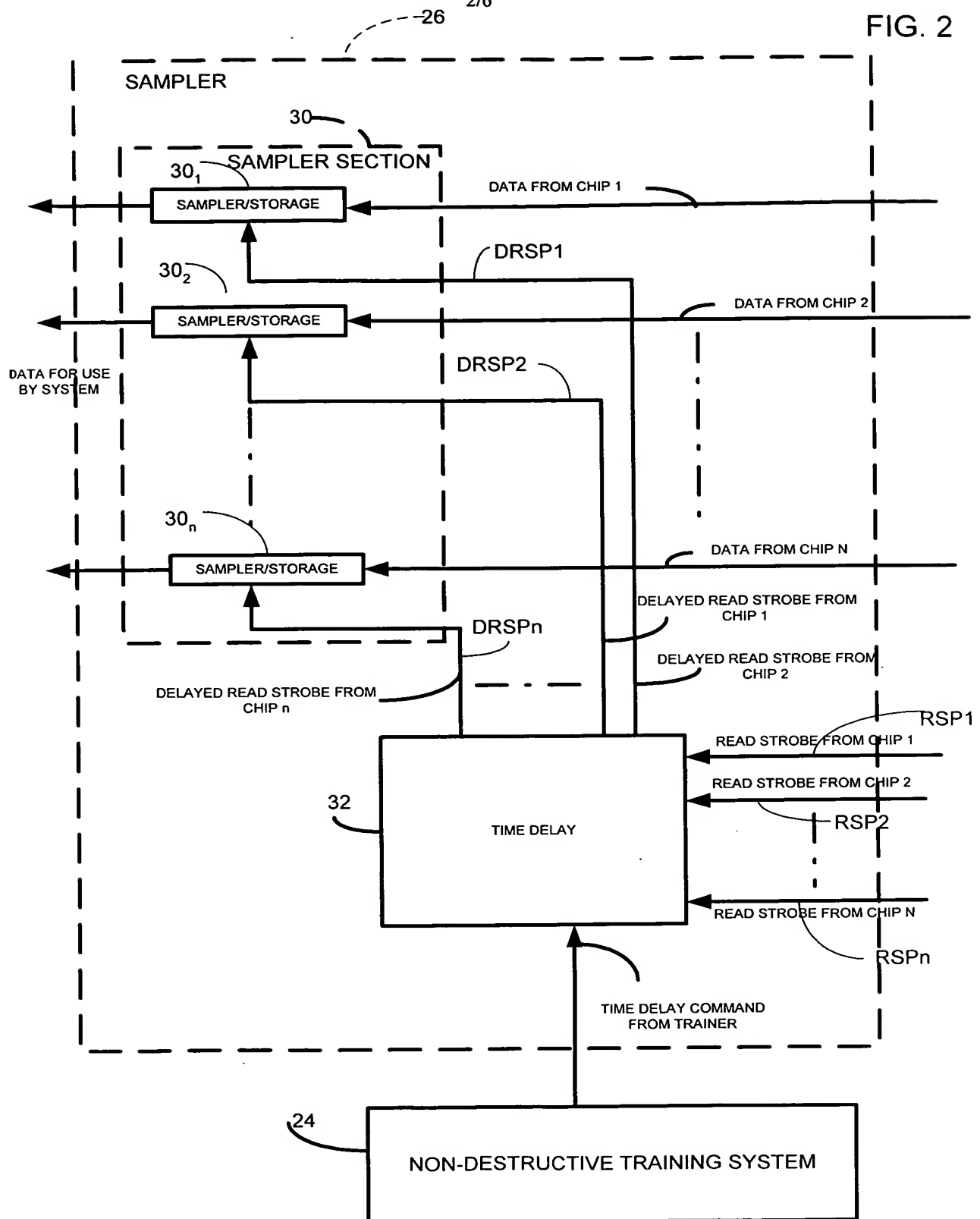
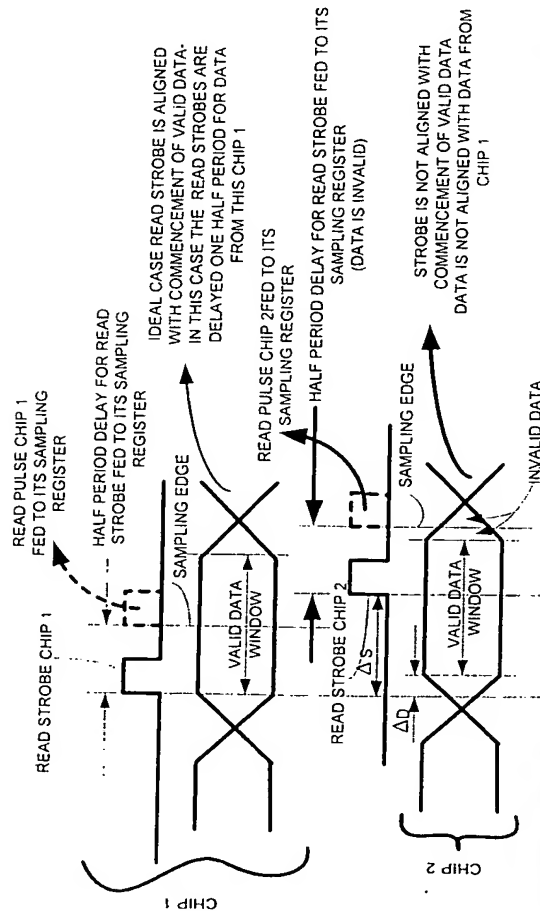
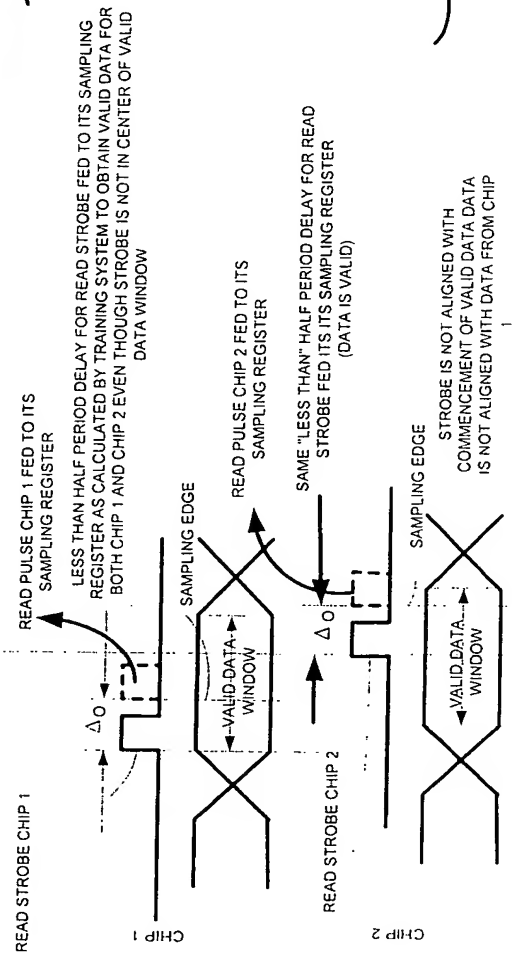


FIG. 2A



WITHOUT TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES INVALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2

FIG. 2B



WITH TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES VALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2

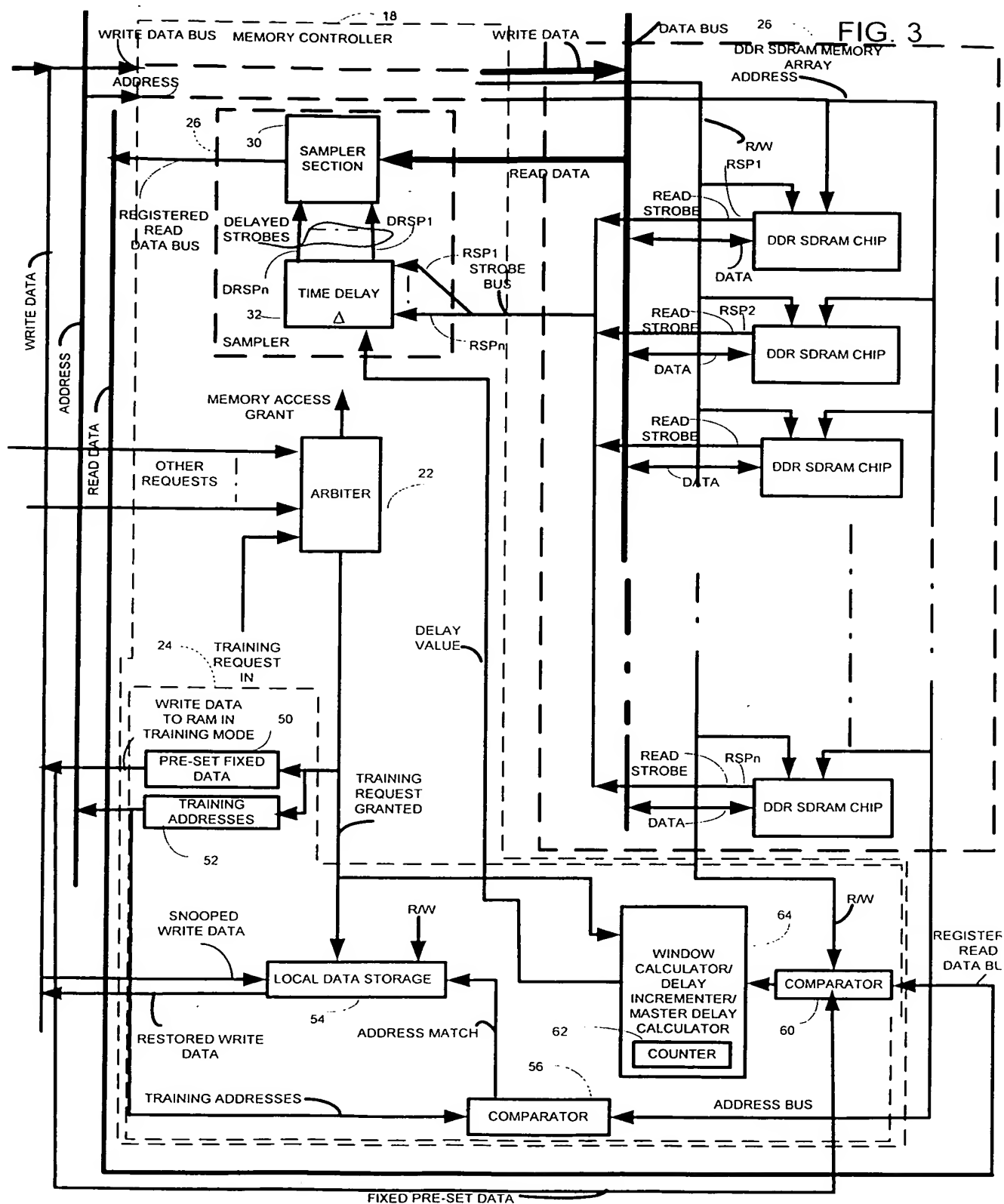


FIG. 4

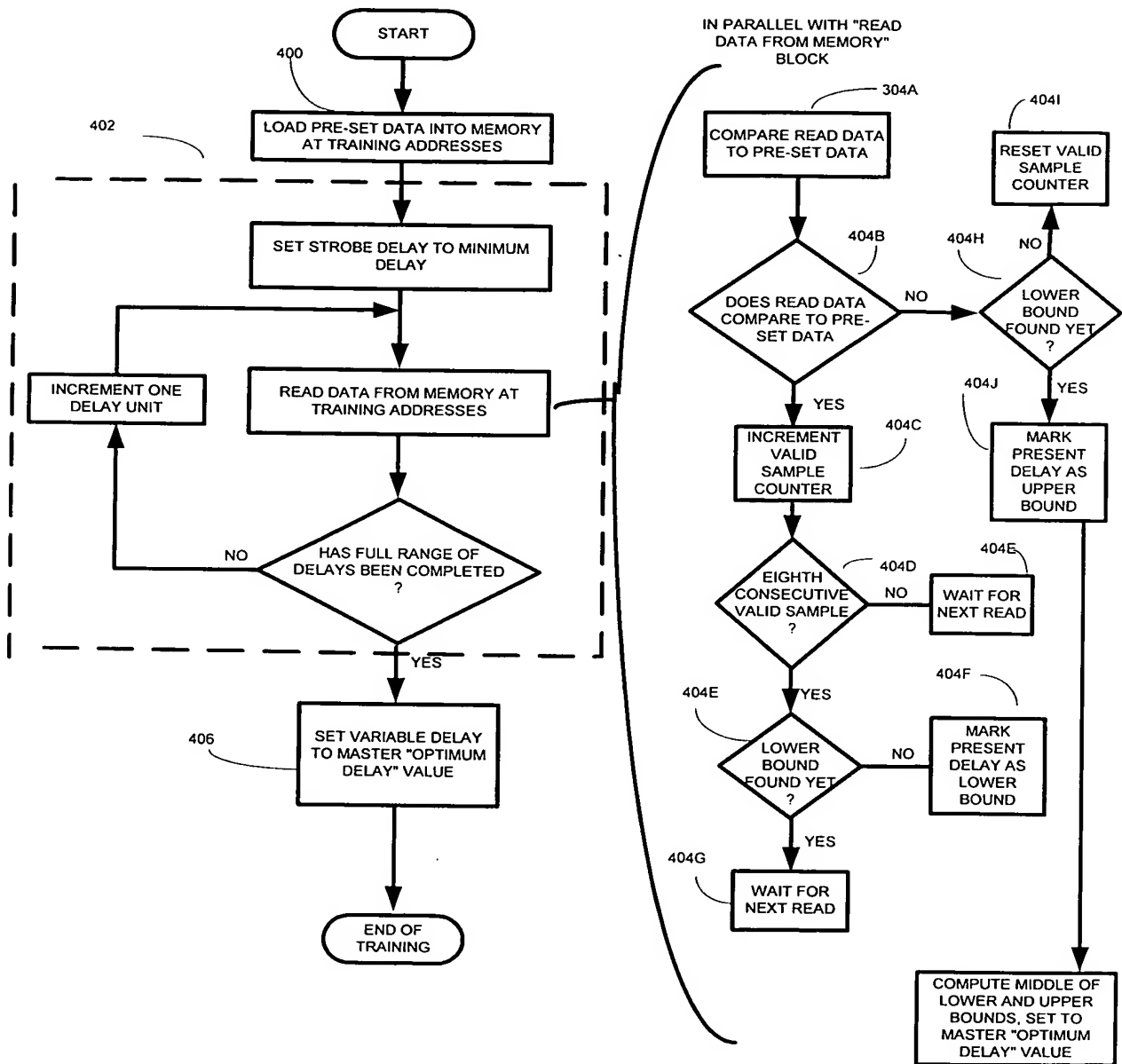


FIG. 5

